Remarks

Claim Rejections Under 35 USC 103(a)

Claims 34-35, 39-41, 43, 49 and 51 have been rejected under 35 USC 103(a) as being unpatentable over Fjelstad et al. (US Patent No. 5,615,824) in view of Maruyama et al. (US Patent No. 6,661,247).

Claim 38 has been rejected under 35 USC 103(a) as being unpatentable over Fjelstad et al. (US Patent No. 5,632,631) and Maruyama el a. (US Patent No. 6,661,247) in view of Sugiyama et al. (US Patent No. 4,766,666).

Claims 40-41 and 50 have been rejected under 35 USC 103(a) as being unpatentable over Fjelstad et al. (US Patent No. 5,632,631) and Maruyama et al. (US Patent No. 6,661,247) in view of Kazle (US Patent No. 5,936,847).

The rejections under 35 USC §103 are traversed for reasons to follow.

Reading of Claims

Following is a claim chart reading the amended claims on the drawings and specification.

34. A method for fabricating an interconnect 10 for electrically engaging a semiconductor component with a least one bumped contact comprising:	interconnect 10, pg. 9, lines 6-30 semiconductor component 18 bumped contact 14B	Fig. 1 Fig. 3B Fig 7G
providing a substrate having a	substrate 14B, pg. 18, line 33 - pg. 19, line 3	Fig. 7A
first surface and a	first surface 26B	Fig. 3C
second surface;	second surface 44B	Fig. 3C
forming a plurality of leads	leads 22B, pg. 19, lines 10-14	Fig. 7C
on the first surface	surface 26B	Fig. 3C
configured to electrically engage and support the bumped contact, the leads having terminal portions and support portions connected by a connecting segment;	14B, pg. 4, lines 18-21 connecting segment 40B, pg. 19, lines 11-14	Fig. 3B Fig. 7G Fig. 7G Figure 7I
forming a recess in the first surface at least partially encircled by the connecting segment configured to support and cantilever the terminal portions over the recess for movement within the recess during electrical engagement of the bumped contact; and	recess 20B, pg. 21, lines 10-14 pg. 21, lines 12-14 pg. 13, lines 5-8	Figure 7F
forming an opening through the connecting segment and the substrate to the second surface;	opening 60D, pg. 19, lines 15-17	Fig. 7D
depositing a conductive material in the opening; and	conductive material 66B, pg 20, lines 8-9	Fig. 7E
forming a contact on the second surface in electrical communication with the conductive material.	contact 38B, pg. 20, lines 32-33	Fig 7E
35. The method of claim 34 further comprising forming outer layers on the terminal portions configured to provide a non bonding surface for the bumped contact.	layers 46B, pg. 19, lines 4-9	Figs. 7B & 3D
38. The method of claim 34 wherein the substrate comprises a semiconductor material and further comprising forming an insulating layer in the opening prior to the depositing the conductive material step.	pg. 10, line 4 insulating layer 24B, pg. 19, lines 32-33	Fig. 7D

39. A method for fabricating an interconnect for electrically engaging a semiconductor component having at least one bumped contact comprising:	interconnect 10, pg. 9, lines 6-30 semiconductor component 18 bumped contact 14B	Fig. 1 Fig. 2C Fig. 7G
providing a substrate having a	substrate 14B, pg. 18, line 33 to pg. 19, line 3	Fig. 7A
first surface and a	first surface 26B	Fig. 3C
second surface;	second surface 44B	Fig. 3C
forming a plurality of leads on the first surface configured to electrically engage and support the bumped contact, the leads having terminal portions and support	leads 22B, pg 19, lines 10-14	Fig. 7C Fig. 7G
portions connected by a connecting segment;	connecting segment 40B, pg 19, lines 11-14	Fig. 7I
forming a recess in the first surface at least partially encircled by the connecting segment configured to cantilever the terminal portions over the recess for movement within the recess during electrical engagement of the bumped contact; and	recess 20B, pg. 21, lines 10-14 pg. 21, lines 12-14 pg. 13, lines 5-8	Fig. 7F
forming an opening through the connecting segment and the substrate to the second surface;	opening 60D, pg. 19, lines 15-17	Fig. 7D
forming an insulating layer in the opening; and	insulating layer 24B, pg. 19, lines 32-33	Fig. 7D
depositing a conductive material in the opening.	conductive material 66B, pg. 20, lines 8-9	Fig. 7E
40. The method of claim 39 further comprising shaping the terminal portions with a curvature matching a shape of the bumped contact.	pg. 21, lines 18-20	
41. The method of claim 39 further comprising forming a contact on the second surface in electrical communication with the conductive material.	contact 38B, pg. 20, lines 32-33	Fig. 7E
43. The method of claim 39 further comprising forming a second insulating layer in the recess.	second insulating layer 24B, pg. 19 lines 32-33	Fig. 7D
49. A method for fabricating an		

interconnect for electrically	interconnect 10, pg. 9, lines 6-30	Fig. 1
engaging a semiconductor	semiconductor component 18, pg. 9	Fig. 2C
component having a plurality of	lines 6-30	
bumped contacts comprising:	bumped contacts 16, pg. 9,	Fig. 2C
	lines 6-30	
providing a substrate having a	substrate 14B, pg. 18, line 33 to	Fig. 7A
	pg. 19, line 3	
first surface and a	first surface 26B	Fig. 3C
second surface;	second surface 44B	Fig. 3C
forming a plurality of interconnect	interconnect contacts 14B, pg 18,	Fig. 7G
contacts on the first surface	line 2 to pg. 21, line 20	
configured to electrically engage the		
bumped contacts, each interconnect	bumped contacts, pg. 9, line 26	
contact comprising a plurality of leads	22B, pg 19, lines 10-14	Fig. 2C
having terminal portions and a	terminal portions 30A, pg. 10, line33	Fig. 2B
connecting segment on the first	connecting segment 40B, pg 19,	Fig. 7I
surface connecting the leads;	lines 11-14	
forming outer layers on the terminal	outer layers 46B, pg. 19, lines 4-9	Figs. 7B & 3D
portions configured to provide non-		
bonding surfaces for the bumped		
contacts;	pg. 13, line 27, to page 14, line 2	
forming a plurality of recesses	recesses 20B, pg. 21, lines 10-14	Fig 7F
in the first surface, each recess at		
least partially encircled by a		
connecting segment, the recesses		
configured to cantilever the terminal		
portions of the leads for movement		
within the recesses during electrical		
engagement; and	pg. 12, lines 2-5	
forming a plurality of conductive	conductive vias 42B, pg. 13,	Fig. 7E
vias in the connecting segments and	lines 16-17	
in the substrate from the first		
surface to the second surface; and		
forming a plurality of contacts on	contacts 38B, pg. 20, lines 32-33	Fig. 7E
on the second surface in electrical		
communication with the conductive		
vias.		
50. The method of claim 49 wherein		
the forming the conductive vias step		
comprises forming an opening	opening 60D, pg. 19, lines 15-17	Fig. 7D
through each connecting segment and		
depositing a conductive material.	conductive material 66B, pg. 20,	Fig. 7E
	lines 8-9	
51. The method of claim 49 further		
comprising forming projections on	projections 28B	Fig. 7B
the leads prior to the forming the		
outer layers step.		

Argument

The claims have been amended to include additional limitations which overcome the rejections, and further distinguish the claimed method from the prior art. In particular, the independent claims (34, 39, 49) have been amended to state that the substrate 12B (Figure 7A) includes a first surface 26B (Figure 3C) and a second surface 44B (Figure 3C).

Amended independent claim 34 recites the step of forming leads 22B (Figure 7I) which include a connecting segment 40B (Figure 7I). In addition, claim 34 recites the step of forming a recess 20B (Figure 7F) in the first surface at least partially encircled by the connecting segment 40B. Claim 34 also recites the step of forming an opening 64B (Figure 7D) in the connecting segment 40B and through the substrate 12B (Figure 7D). Claim 34 also recites the step of depositing a conductive material 66B (Figure 7E) in the opening 64B, and forming a contact 38B (Figure 7E) on the second surface in electrical communication with the conductive material 66B. These steps provide a conductive via 42B (Figure 7G), and a back side contact 38B (Figure 7G) which allow signals to be transmitted through the substrate 12B (Figure 7G) to the interconnect contact 14B (Figure 7G). In addition, the leads 22B are cantilevered over the recess 20B (Figure 7F), which functions to center and retain the bumped contact 14B (page 11, line 27). Amended independent claims 39 and 49 include similar recitations.

In Fjelstad et al. contact tabs 20 (Figure 2) are mounted to a connector body 40 (Figure 2) which functions as a substrate. The connector body 40 (Figure 2)

incorporates a sheet-like, metallic element having holes 46 therein (Figure 2, column 8, lines 38-39). In addition, conductive metallic via liners 52 are formed in the holes 46 (Figure 2, column 8, lines 43-45).

In Fjelstad et al. there is no recess forming step, because there are no recesses. Rather, the contact tabs 20 are mounted over holes 46 on the connector body 40. In addition, openings are not formed through both the contact tabs 20 and the connector body 40 as presently claimed. Rather, the connector body 40 includes the holes 46, and the contact tabs 20 are formed on a sheet, which is laminated to the connector body in alignment with the holes (Figure 7, column 11, lines 49-51).

The present method forms a simpler structure, which does not require an alignment and laminating step as in Fjelstad et al. Rather, the openings 64B (Figure 7D) for the conductive vias 42B (Figure 7E) can be formed using a self aligning technique, such as laser machining through both the connecting segment 40B and the substrate 14B (page 19, lines 15-18). In addition, the present method provides a recess 20B, which improves the performance of the interconnect contact 14B, because the recess 20B centers and retains the bumped contact 14B.

Amended independent claim 39 (and dependent claim 38) also recite that the substrate comprises a semiconductor material, and recite the step of forming an insulating material in the opening. In contrast, Fjelstad et al. teaches a metal substrate (i.e., metallic connector body 40). In support of the rejections, Sugiyama was cited as teaching a semiconductor material, and was combined with Fjelstad et al. The proposed motivation for the combination is stated in paragraph 4 of the Office Action

as: "providing a semiconductor material, as taught by Sugiyama, for the purpose of electrically communicating between two surfaces using the semiconductive material instead of metal".

However, the semiconductor substrate in the present method is not used for electrical communication, but rather as a material which has the same CTE as the semiconductor components being tested (page 4, lines 13-15). Similarly, in Fjelstad et al., the metallic connector body 40 is not used for electrical communication, but must be electrically insulated to prevent conduction (column 8, lines 39-41). The proposed motivation of using a semiconductor for electrical communication for the combination of Sugiyama and Fjelstad et al., is thus not plausible.

The step of shaping the leads has been removed from the independent claims, but has been included in amended dependent claim 40. This feature is submitted to be unobvious for essentially the same reasons advanced in the Amendment dated April 26, 2005. Specifically, one skilled in the art at the time of the invention would have no incentive to combine Maruyama et al. and Fjelstad et al. in the manner of the Office Action.

The step of forming a non bonding surface on the leads as recited in dependent claim 35, is also submitted to be unobvious for essentially the same reasons advanced in the Amendment dated April 26, 2005. Specifically, one skilled in the art at the time of the invention would have no incentive to combine Kazle and Fjelstad et al. in the manner of the Office Action.

Conclusion

In view of the amendments and arguments, favorable consideration and allowance of claims 34, 35, 38-41, 43 and 49-51 is respectfully requested. In addition, rejoinder of withdrawn dependent claims 36, 37, 42 and 52 is requested. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

DATED this 8th day of September, 2005.

Respectfully submitted:

STEPHEN A. GRATTON
Registration No. 28,418
Attorney for Applicant

2764 S. Braun Way
Lakewood, CO 80228
Telephone: (303) 989-6353
FAX (303) 989-6538

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, PO BOX 1450, Alexandria, VA 22313-1450 on this 8th day of September, 2005.

September 8, 2005
Date of Signature

Stephen A. Gratton, Attorney for Applicant